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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Morgan

Art Unit: 2674

Serial No.: 09/088,674

Examiner: Nguyen, Kevin M.

Filed: 2 June 1998

Docket No. TI-25995

For: BOUNDARY DISPERSION FOR ARTIFACT MITIGATION (as amended)

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NAME OF INVENTOR(S): Morgan	RECEIPT DATE & SERIAL NO.: Application No.: 09/088,674
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Applicant: Morgan — Art Unit: 2674

Serial No.: 09/088,674 — Examiner: Nguyen, Kevin M.

Filed: 06/02/1998 — Docket No. TI-25995

For: BOUNDARY DISPERSION FOR ARTIFACT MITIGATION

REPLY BRIEF

16 March 2007

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Charles A. Brill — 16 March 2007 (Date)

Dear Sir:

In response to the Examiner's Answer mailed 16 January 2007, applicant responds as follows:

REMARKS

Claim 1:

The Examiner stated, "Yamaguchi et al teach . . . a first pixel value defined by [(3V) is mean effective voltage], see fig. 7B." The information bracketed by the Examiner is at issue. The applicant respectfully submits that the Examiner fails to understand the teachings of Yamaguchi.

Figures 5 though 7D of Yamaguchi illustrate the problem solved by Yamaguchi—namely how to display more grey levels than one has voltage levels to drive an LCD panel. Normally, in order to drive four grey levels on an LCD panel, four voltage levels would be required, and the

data driver would select the appropriate voltage level for each pixel based on the pixel's grey level value. Yamaguchi teaches that by dividing a display period into two fields, and intelligently altering the bias voltage levels, a given pixel value can select bias voltages that drive the panel to an average grey level that is equivalent to a constant bias voltage other than the few voltages available.

In Figure 5, Yamaguchi provides a transmission curve showing four gray levels that equate to bias voltages of 2, 3, 4 and 5 volts. In Figure 6, Yamaguchi shows that one frame may be produced as two fields. In Figure 7A, Yamaguchi shows how "Grey-Scale Level 1" can be produced by two fields in which a 2 volt bias is selected during the first field and a 2 volt bias is selected during a second field. In Figure 7B, Yamaguchi shows how "Grey-Scale Level 2" can be produced by two fields in which a 2 volt bias is selected during the first field and a 4 volt bias is selected during a second field. In Figure 7C, Yamaguchi shows how "Grey-Scale Level 3" can be produced by two fields in which a 6 volt bias is selected during the first field and a 2 volt bias is selected during a second field. In Figure 7A, Yamaguchi shows how "Grey-Scale Level 4" can be produced by two fields in which a 6 volt bias is selected during the first field and a 4 volt bias is selected during a second field.

As a result, only two voltages (2 and 6) need to be supplied to the LCD panel during the first field, and only two voltages (2 and 4) need to be supplied to the LCD panel during the second field. The pixel values driving the data drivers enable the proper voltages to be driven to the panels. Yamaguchi doesn't appear to explain the bias voltage selection process with respect to Figure 7. Figure 22, however, suggests the pixel value could be used as a digital input and decoded to select a drive voltage. For example, Yamaguchi's four grey scale values can be

represented by a 2-bit binary grey-scale pixel value. The MSB could select either the 2 volt or 6 volt input during the first field, while the LSB could select either the 2 volt or the 4 volt input during the second field. In this manner, the pixel value (binary 11, 10, 01, 00 for gray-scale values 4, 3, 2, 1) is never changed, but is used to select a bias voltage.

The applicant reiterates that Yamaguchi doesn't appear to explain the bias voltage selection process with respect to the first embodiment shown in Figure 7. The Examiner has not attempted to explain this aspect of the teachings of Yamaguchi. Given Yamaguchi's teaching that the A/D conversion portion (9) quantizes each color with two bits, which are divided and output separately as one bit signal for each color for each field (see Figure 1A, 1B, and lines 28-55 of column 6 of Yamaguchi), the foregoing is one plausible explanation.

Returning to the Examiner's analysis of Claim 1 in view of the teachings of Yamaguchi, the Examiner's statement that Yamaguchi's "first pixel value" is "defined by [(3V) is mean effective voltage]" shows the error of the Examiner's application of the teachings of Yamaguchi to Claim 1. Claim 1 recites "offsetting a first pixel value." The Examiner, by the use of the square brackets in the quoted statement, appears to acknowledge that Yamaguchi doesn't ever have a 3 volt pixel value.

The Examiner's argument appears to be that one of ordinary skill would realize that Yamaguchi created a pixel using alternate bias voltages of 2 and 4 volts, decide that Yamaguchi therefore inherently possessed a 3 volt pixel value but rather than use the 3 volt pixel value inherently offset the (virtual) 3 volt pixel value by a+/- 1 volt to obtain the 2 and 4 volt signals actually utilized by Yamaguchi. This appears to ignore the teachings of Yamaguchi which claim to be able to create additional gray-scale levels without increasing the complexity of the drive

circuit normally associated with providing additional bias voltages (see columns 1 through line 45 of column 2 of Yamaguchi).

The applicant submits that none of the voltages shown in Figure 7 should be considered a pixel value, but rather they are the bias voltages selected to drive the various pixels of the LCD panel in response to pixel values that represent the desired gray scale level.

If the Examiner's application of the label "pixel value" to the voltages shown in Figure 7 is accepted, the Examiners analysis fails because there is no "3V" pixel value. Therefore, the 3V signal cannot be offset "a first predetermined amount to form a first offset pixel value," much less offset "by the opposite of said first predetermined amount to form a second offset pixel value" as required by Claim 1. 3V may indeed be a mean effective voltage of the two bias voltages, but it is not a pixel value that is offset to obtain the two offset pixel values as required by Claim 1.

If the Yamaguchi's pixel value is considered to be the 2-bit "digital display data" digitized by A/D conversion portion (9) which, after formatting by data conversion portion (10) and parallel conversion portions (11 and 12), are extracted from field memories (13 and 14) and used as an input to the data drivers (8) of Figure 1B of Yamaguchi (see Figure 1A, 1B, and lines 28-55 of column 6 of Yamaguchi), the Examiner's rejection fails because Yamaguchi does not show, teach, or suggest the offsetting limitation of Claim 1.

Claim 6:

The Examiner stated, "Yamaguchi et al inherently teach a logic circuit defined by means for offsetting inherently a first predetermined amount '-1' [defined by an area hatching from 3V to 2V at the first field] to form a first offset pixel value [defined by 2V at the first field]."

The applicant respectfully submits this argument inherits the flaws described above with respect to Claim 1. Namely, that the virtual 3V signal cannot be considered a pixel value that is offset, much less that any circuit shown, taught, or suggested by Yamaguchi actually offsets this pixel value.

The Examiner stated, "the examiner finds that Yamaguchi inherently teaches the average circuit corresponding to the logic circuit that performs the corresponding function that is similar to those of claim 1, though in apparatus form, therefore the rejection of claim 6, will be treated using the same rationale as recited in claim 1."

The applicant respectfully submits that the Examiner's logic is not proper. Whether Yamaguchi teaches, inherently or not, an average circuit is irrelevant to this analysis. Yamaguchi, as discussed above with respect to Claim 1, does not offset a pixel value and furthermore does not show, teach, or suggest "a logic circuit offsetting a first pixel value" as recited by Claim 6.

Claims 2 and 7:

The Examiner stated, "a person of ordinary skills in the mathematic and Yamaguchi inherently teaches said first predetermined amount '-1' defined by 2V-3V at the first field, said predetermined amount '+1' defined by 4V-3V at the first field. Thus, said first predetermined amount '-1' and '+1' is selectively as a function of (X-3), where X is equal to 2V, and X is equal to 4V."

Claims 2 and 7 recite "the value of said first predetermined amount" is selected "as a function of said first pixel value." The applicant respectfully submits while it is unclear what the Examiner is trying to convey, the Examiner has failed to present a prima facie rejection of

Claims 2 and 7.

Claims 3 and 8:

The Examiner stated, "Yamaguchi inherently teaches said first offset pixel value 2V is less than said first pixel value (3V) as a function of (X-3) of the spatial location '-1' defined the spatial location and (3V) is mean effective voltage defined to be displayed. Therefore, the first dimension '-1' to concentrate on is the spatial location as claimed."

Claims 3 and 8 recite "said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed." The applicant respectfully submits while it is unclear what the Examiner is trying to convey, the Examiner has failed to show any relationship to the spatial location of a displayed pixel, much less presented a prima facie rejection of Claims 3 and 8.

Claims 4 and 9:

The applicant respectfully submits that the Examiner's analysis and rejection of Claim 4 and 9 ignores the words of the claim. Specifically, "wherein said first pixel values close to a bit transition of said bit-planes are offset" as recited by Claims 4 and 9.

Response to Examiner's Arguments:

The Examiner quotes Section 2131 of the MPEP. The first two paragraphs of the indented quote appear to the applicant to be irrelevant.

The third paragraph of the indented quote states "Since only the alleged distinction between appellant's claims and reference is recited in functional language, it is incumbent upon appellants, when challenged, to show that the device disclosed by reference does not actually possess such characteristics. See In re Ludtke, 169 USPQ 563 (CCPA) 1971).

The applicant respectfully submits this is not a quote from Section 2131 of the MPEP but rather is the Examiner's own gross mischaracterization of In re Ludtke. In re Ludtke states, "Additionally, where the Patent Office has reason to believe that a functional limitation asserted to be critical for establishing novelty in the claimed subject matter may, in fact, be an inherent characteristic of the prior art, it possesses the authority to require the applicant to prove that the subject matter shown to be in the prior art does not possess the characteristic relied on." 441 F.2d at 664. The applicant submits that Ludtke dealt with two parachutes that were each fabricated by a plurality of circumferentially complete panels separated by a plurality of radially extending lines which Ludtke claimed resulted in a sequential opening. After the Examiner presented a prima facie case of anticipation, Ludtke failed to rebut the Examiner's arguments and instead admitted that the same functional result "may be achieved" by the cited reference.

Here we do not have similar structures or functions much less a showing by the Examiner of similarity. Taken in the abstract—without reference to a rejected claim—the reference to Ludtke is unclear. If applied to the Examiner's rejection of the Claim 1, in which the Examiner claimed each step and element was inherent, Ludtke does not appear relevant as it did not address a method claim, but rather a structure claim in which the disclosed and prior art structures were nearly identical and logically would operate in a similar manner. If applied to the Examiner's rejection of Claim 6, Ludtke does not appear relevant as the Examiner has failed to show structures in Yamaguchi structurally similar to the applicant's "logic circuit offsetting a first pixel value."

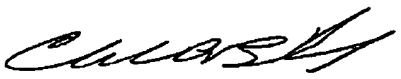
The third paragraph of the Examiner's indented quote further states, "The burden on appellant to rebut an inherency rejection applied to product and process claims. See In re Best,

195 USPQ 430, 433 (CCPA 1977)." The applicant respectfully submits this is not a quote from Section 2131 of the MPEP. In Best, the appealed claim recited a cooling rate that the Examiner and the court believed to be the normal rate resulting from removal of the heat source.

The fourth paragraph of the Examiner's indented quote includes quotes of three references. The applicant respectfully submits this is not a quote from Section 2131 of the MPEP, and furthermore none of the quotations are accurate and none should be relied upon. The first reference is completely misquoted. The citation to the second reference includes a quoted headnote (not part of the court decision) and a misquote from the decision. The citation to the third reference in inaccurate.

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-10 is improper, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejection.

Respectfully submitted,



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